

Design and Simulation of Telescopic Operational Amplifier in 180nm CMOS Technology

Dejan Mirković, Milena Stanojlović Mirković, and Vladimir Petrović

Abstract – This paper presents one approach of designing the single-ended telescopic operational amplifier targeting the 180nm CMOS process node. The proposed solution is suitable for base-band analogue signal processing applications such as moderate rate analogue-to-digital converters and switch-capacitor loop filters of $\Delta\Sigma$ modulators. The design is fully verified for process, voltage and temperature variations.

Keywords - Analogue IC, Operational amplifiers, CMOS technology, Slew-rate, High-gain.

I. INTRODUCTION

The operational amplifiers (opamps) always have played the central role in a realm of analogue signal processing. This is even more pronounced when Application Specific Integrated Circuit (ASIC) is chosen for implementing analogue signal processing functions. All initial, system level, considerations rely on the assumption that this, basic building block, with nearly infinite low-frequency gain and input impedance is readily available. Besides these, first order requirements, more severe constraints may be imposed on the opamp depending on the concrete application.

One may argue that there is almost no room for further exploration when looking back at more than seventy years of active research and development in the field spanning from the vacuum tubes era and invention of opamps (1940's [1]), over the first monolithic realization and commercialization in bipolar (1950's, [2]) and, later on, mos (1970's, [3]) technologies to current times, where majority of industry and academic resources are aimed to realizations in CMOS technology [4].

Regardless of the field maturity, the research in analogue signal amplification is still vigorous. This inherently comes from the very nature of the processed signals enabling the wide spectre of applications (biomedical, data-acquisition and sensing, baseband and RF, etc.). Also, the advances in semiconductor materials and fabrication techniques opened the opportunities for integration of, traditionally non-electronic, signal conditioning concepts with mature solid state semiconductor realization of supporting electronics circuitry. This led to emerging fields like silicon-phonic, on-chip Micro-Electro-Mechanical-Systems and

Dejan Mirković and Milena Stanojlović Mirković are with the University of Nis, Faculty of Electronic Engineering, Aleksandra Medvedeva 4, 18104 Nis, Serbia, E-mail: dejan.mirkovic@elfak.ni.ac.rs, milena.stanojlovic.mirkovic@elfak.ni.ac.rs

Vladimir Petrović is with the Capgemini LLC Belgrade, Analog Design Group Lead, Bulevar Mihajla Pupina 115G, 11000 Belgrade, Serbia, E-mail: vladimir.petrovic@capgemini.com

quantum computing. For these applications, usually there is a hard-constraint on the power consumption while demanding the decent gain and bandwidth. Therefore, achieving this goal in a minimal number of amplification stages (ideally one), is always an attractive option.

Even though, the designer's first choice in these situations is folded-cascode (FC) topology, in this work the single stage, single-ended, telescopic (TC) topology is adopted, regardless of the input/output common-mode range limitations. Since the target application for this work is base-band signal processing for moderate rate analogue-to-digital conversion (ADC) and/or switched-capacitor (SC) filters, where the signal swing is limited, the TC topology will serve well for this purpose. Some of the latest research supports these trends. The authors of [5] published the result based on two stage TC structure that provides 120dB open loop gain and 370MHz unity gain frequency (UGF) with static power consumption of 100 μ W. Of course, this is achieved at the cost of transient response (slew-rate in sub 0.5V/ μ s range). Another interesting solution, based on the modified TC topology, with signal-range dependent programmable gain, is published in [6]. The goal of this work is similar i.e. to extract as high as possible DC gain from a single stage TC opamp without compromising the speed and power consumption performances significantly.

The paper is organized in five sections. In the second section brief discussion and analysis of the TC topology will be covered. The key design equations will be given and explained as well. The third section will outline the design procedure and chosen methodology for sizing the devices. In the fourth section simulation results will be presented and discussed. The findings and conclusions regarding the proposed design will be given in the final, fifth, section.

II. TOPOLOGY ANALYSIS

The core of the single-ended, NMOS-input, TC topology is shown in Fig. 1. The transistors M1 and M2 form the differential input pair which serves as a transconductance stage. Functionally, the $V_{INP} - V_{INM}$, voltage difference is converted into the variations of the drain currents of M1 and M2. The variation of M1's current is mirrored to the right branch and summed with the variation of the M2's current at the output node (V_{OUT}). Mirroring of the M1's current variation is done by employing the M7 and M8 current mirror. Finally, the output voltage is formed by integrating the current variation of the transconductance stage at the output

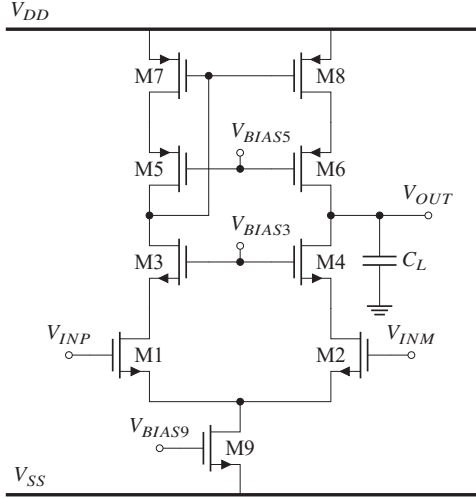


Fig. 1. Telescopic core topology

capacitive load, C_L .

The role of the transistors M3 to M6 is to increase the small-signal resistance at the output node (output resistance) by means of the series-series negative feedback. One should note that the transistors M5 to M8 form a high swing, cascode, current mirror where M7 is diode connected indirectly through M5. Transistor M9 serves as the constant current source that provides necessary DC biasing of the whole TC topology (tail current source).

The DC bias voltages, V_{BIAS3} and V_{BIAS6} , should be generated in a such way to support saturation mode of operation for all transistors under maximal input/output voltage swings and all process, voltage and temperature corners (PVT). In order to relate the design requirements and constraints with the circuit parameters, small-signal analysis is performed next. Since the results of the small signal analysis will serve as the guideline for the initial calculations and qualitative consideration, one should note that the given results are heavily approximated. For the same reasons and ease of analysis, but without loss of generality, it is assumed that the transistors M1 to M8 have the same size.

First, let's consider the low-frequency i.e. DC gain for small signals. This parameter is easily obtained when the output resistance and total transconductance of the circuit is known. As described in the first paragraph of this section, by idealizing the current mirror, it is evident that the total transconductance coincides with the transconductance of the transistors M1 and M2. Therefore, $G_m = g_{m1,2}$. On the other hand, knowing that the series-series negative feedback will increase the single transistor intrinsic, small-signal, resistance, r_{ok} , where $k = 1, 2, 7, 8$, by the factor of one plus the loop gain which, in a case of the cscode structure equals, $1 + g_{m,k}r_{o,k}$, where $k = 3, 4, 5, 6$, total output resistance for the differential input signal is $R_o \approx (g_{m4}r_{o4}r_{o2}) \parallel (g_{m6}r_{o6}r_{o4})$, assuming, $g_m r_o \gg 1$. Small-signal, DC gain is then, $A_o = G_m \times R_o$. This is one of the advantages of the TC topology, i.e. it gives high DC gain in

one stage by design.

Taking into account the dominant parasitic capacitances of transistors, the most influential poles and zeros of the TC topology are,

$$\omega_{p1} \approx 1/R_o C_L, \quad (1)$$

$$\omega_{p2} \approx \omega_{T3,4}/3, \quad (2)$$

$$\omega_{p3} \approx 3\omega_{T7,8}/2, \quad (3)$$

$$\omega_{z1} \approx \omega_{T7,8}, \quad (4)$$

where $\omega_T = g_m/C_{GG} = 2\pi f_T$ is the transient, angular, frequency of the transistor and C_{GG} total gate capacitance. The ω_{p1} is the dominant pole (the closest to zero frequency). Based on (1) the unit-gain-frequency (UGF) is,

$$\omega_u = A_o \omega_{p1} \approx g_{m1,2}/C_L. \quad (5)$$

The non-dominant poles and left-half-plane zero ω_{z1} should be at relatively high frequencies i.e. the TC is inherently stable (self-compensated with the loading at the output). However, in practical realization, this commodity may easily be lost if the transistors M4 to M8 becomes large due to, usually, transient requirements. This is especially true for the current mirror pole-zero doublet $[\omega_{p3}, \omega_{z1}]$.

Being a cascode stage, TC structure provides solid Power-Supply-Rejection-Ratio (PSSR). Applying the small-signal excitation at the positive/negative power supply line, V_{DD}/V_{SS} , one gets,

$$PSSR_{dd} \approx \frac{3}{4} g_{m1,2} r_{o1,2} g_{m4,6} r_{o4,6} \quad (6)$$

$$PSSR_{ss} \approx \frac{3}{4} \frac{g_{m1,2}}{g_{m9}}. \quad (7)$$

Similar is true for the Common-Mode-Rejection-Ratio (CMRR),

$$CMRR \approx 2A_o g_{m8} r_{o5}. \quad (8)$$

As for the thermal noise considerations, TC topology has properties similar to simple 5 transistor single-stage OTA,

$$\bar{v}_{n,out}^2 = \frac{k_b T}{C_L} n_F \quad (9)$$

$$n_F \approx 2A_o \gamma \left(1 + \frac{g_{m7,8}}{g_{m1,2}} \right), \quad (10)$$

where $\bar{v}_{n,out}^2$ is the total, integrated, noise power at the output and n_F is the topology dependent noise factor, γ is technology constant close to 2/3, $k_b \approx 1.38 \times 10^{-23} \text{ J/K}$ is the Boltzmann's constant, and T is the absolute temperature.

The key transient parameter is a slew-rate (SLR) which can be derived by approximate large-signal analysis. Assuming the open loop configuration, this parameter is no different from the above-mentioned, 5 transistors OTA. Basically, if one of the inputs experience the fast ramp signal, while the other stays at common-voltage, the current of the tail current

source M9 will be steered to the side of the active input transistor. This current will further, charging or discharging the output capacitive load, forming the maximal output voltage rate of approximately,

$$SLR \approx \pm I_9 / C_L. \quad (11)$$

As with all approximate analysis, this result should also be taken with the caution. Namely, the current of the tail current source M9 calculated by this criterion may not be sufficient to fulfil the SLR requirement due to the self-loading effect and applied negative feedback which is inevitable in any real application. Therefore, the transient simulation will aid in choosing the right value of the I_9 that will support the required SLR for all working conditions. The choice of the tail current will directly influence the static power consumption of the circuit. Since there are only two branches that will draw significant currents, power consumption is expected to be low by design.

Finally, the true drawback of the TC topology is the input/output common-mode range (I/OCMR) when used in the unity-gain configuration (unity gain buffer - UGB). Relative to bias voltage V_{BISA3} , inverting input of the TC opamp INM (the gate of M2) cannot go above,

$$V_{INM} \leq V_{GS3,4} - V_{BISA3} + V_{TH1,2}, \quad (12)$$

in order to keep M2 in the saturation region. On the other hand, the output node voltage cannot go below,

$$V_{OUT} \geq V_{BISA3} - V_{TH3,4}, \quad (13)$$

since, otherwise, the M4 will go to triode region. To form the unity buffer, the INM and OUT ports of the TC opamp needs to be shorted i.e. $V_{OUT} = V_{IM}$. Combining the (12) and (13) one gets the allowed I/OCMR for the TC in unity buffer configuration,

$$OCMR = V_{TH2} - (V_{GS4} - V_{TH3,4}), \quad (14)$$

where, $V_{GS4} - V_{TH3,4} = V_{ov3,4}$, is basically the overdrive voltage of the M3 and M4. Due to the voltage headroom and transistor efficiency optimization this voltage is always chosen to be smaller than the threshold voltage. This means that, to keep all transistor of the TC UGB in saturation the OCMR is constrained to less than the one threshold voltage. In sub-micron CMOS technologies, where the $V_{TH} \approx 0.5V$ and optimal $V_{ov} \approx 0.2V$, this range is only about $OCMR \approx 0.3V$.

There are techniques to reduce this limitation, like the one suggested in [7] and [8], but these come with the price of higher power consumption and/or lower SLR and UGF. Therefore, in this work we did not address this limitation, especially since our target applications usually require the non unity-gain feedbacks and bounded signal ranges. Our prime focus here is to achieve as high as possible DC gain without significantly degrading the SLR, UGF and power consumption.

III. DESIGN PROCEDURE

The target specifications are: static power consumption less than $500\mu W$, at least 60dB of DC gain with UGF of more than 20MHz, unity-gain stable with at least 45° of phase margin (PM), more than $30V/\mu s$ SLR in both directions and input offset voltage within $\pm 2mV$ range. Estimated capacitive load is up to 2pF. All specs should be fully or nearly satisfied over the process corners, $\pm 10\%$ of power supply voltage variations and industrial temperature range of $-40^\circ C$ to $85^\circ C$.

Since the core TC topology is pretty simple the design procedure is quite forward as well. The design steps are,

- use (5) to calculate the transconductance for a given UGF and capacitive loading;
- use the (11) to estimate the tail current source current for a given SLR and capacitive loading;
- calculate branch currents i.e. the currents of the transistors M1 to M8 by evenly splitting the current of the tail current source, $I_k = I_9/2$ and $k = 1, 2, \dots, 8$.

Now, based on the estimated currents and/or transconductances, the g_m/I_D or inversion coefficient methodology for the device sizing can be applied [9, 10]. The steps are,

- calculate differential pair transistors' efficiencies, $g_{m1,2}/I_{1,2}$, based on needed transconductance and current and adopt the efficiency for transistors M3 to M8 (as a rule of thumb chose 10 for moderate, 5 for deep and 15 for weak inversion);
- carefully consider the role of each transistor in the circuit and chose the appropriate channel lengths based on a experience, reasoning and/or consult the pre-simulated and compiled charts/tables for important small-signal transistor parameters (g_m , r_o , f_T , etc.);
- use the pre-simulated and compiled charts/tables to determine the current densities, I_D/W , for calculated/adopted transistors' efficiencies and chosen channel length from previous steps;
- calculate the needed channel widths based on transistors' currents and current densities.

After a dozen of iterations the final design that meets all the requirements over the PVT corners is achieved. To meet the SLR spec, about $25\mu A$ larger currents per branch were necessary compared to the initially calculated one. Also, rather high channel length of $2\mu m$ proves to be good choice for fulfilling the DC gain spec. This pushed the channel widths to go larger than initially calculated for the typical corner. As a result, transient frequencies of the transistors for the $90\mu A$ to $100\mu A$ current range, drops to 100's of MHz bringing the mirror pole-zero doublet and non-dominant pole closer to the UGF jeopardizing the PM. This is also due

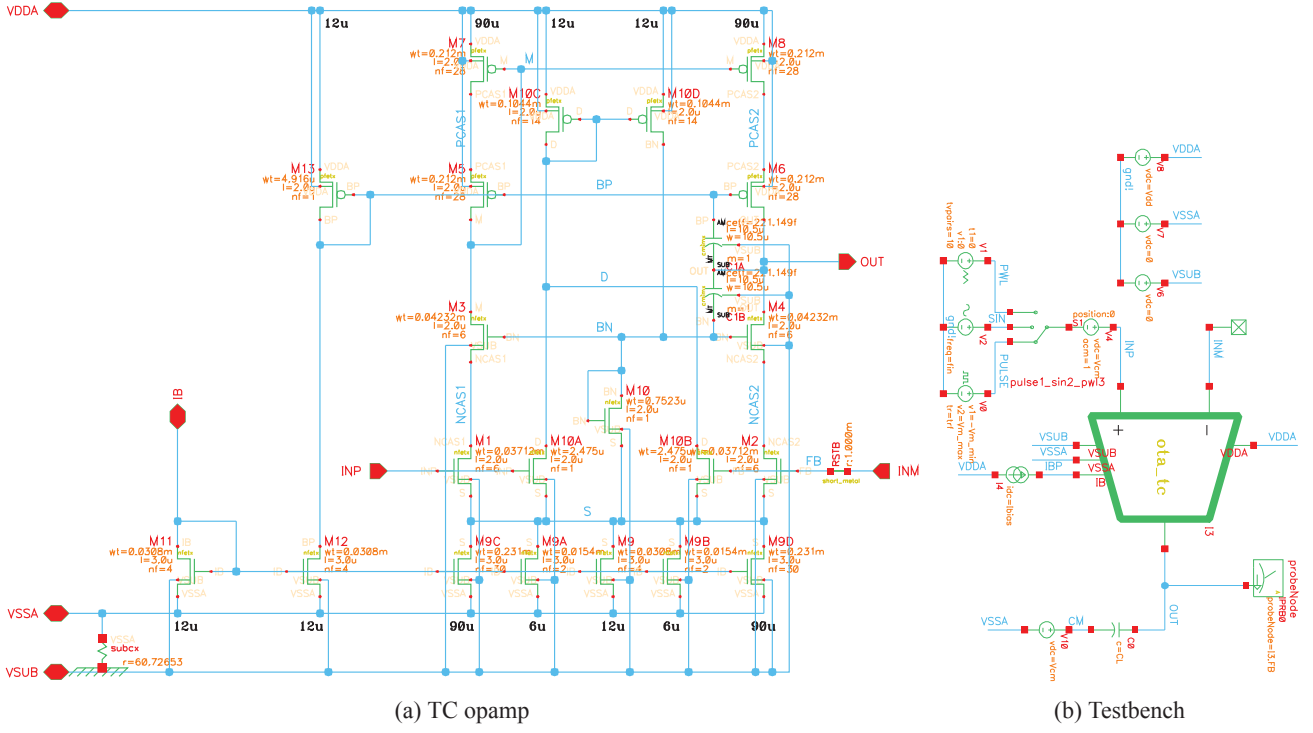


Fig. 2. Schematic and testbench of a telescopic opamp

to the relatively low capacitive load. To counter this, additional pair of about 220fF compensation, Metl-insulator-Mtal (MiM), capacitors are introduced around the output cascode devices, M4 and M6, to lower the gain at high frequencies. This way the required PM of 45° is preserved.

The practical schematics of the designed TC opamp and testbench are shown in Fig. 2. The Fig. 2a shows the detail circuit's schematic with biasing network and annotated component dimensions and branch currents. To better track, and later in the layout phase match, the branch currents main tail current source, M9 in Fig. 1, is split into the two identical instances M9C and M9D which match the currents of M1 and M2, respectively. The same is done for the biasing transistors M10A and M10B which are biased with the tail current sources M9A and M9B. This is again repeated for the floating voltage source (V_{GS} reference) M10 and its tail current source M9. The M10 sets appropriate biasing point for the gates of M3 and M4 (V_{BIAS3} in Fig. 1).

To make M10 actively update the biasing point of the M3 and M4, its drain current is governed by the M10C and M10D mirror. Practically, M10A and M10B behaves as a pseudo differential pair that tracks the input signals. The moment one of the sides starts to switch off i.e. the other to switch on, the current of the M10 will be adjusted by drawing the right amount of current from the M10D to support these input signals changes. This is done by reflecting the input signal changes into the mirrors reference current (transistor M10C) which are mirrored back to M10 over the M10D. The M10 is carefully designed to support max-

imal, open loop voltage swing, i.e. to provide the voltage of $V_{GS3,4} + V_{ov1,2} = V_{TH3,4} + V_{ov3,4} + V_{ov1,2}$ between gates of M3 and M4 and sources of M1 and M2. Similarly, M13 is designed to provide voltage of $V_{GS5,6} + V_{ov7,8} = |V_{TH5,6}| + V_{ov5,6} + V_{ov7,8}$. Transistors M11 and M12 serve to mirror the reference current from the external stable source into the TC opamp's biasing network.

Testbench for the closed loop, unity-gain, verification is given in Fig. 2b. In the testbench, three types of the excitation generators are available: pulse, piecewise linear and sinusoidal. The DC gain, UGF and PM are extracted from the stability analysis, while the SLR is calculated from the pulse excitation. Offset voltage is calculated from DC analysis as a voltage difference between INM (OUT) and INP ports. Results are given in the next section.

IV. SIMULATION RESULTS

In the ams AG's 180nm CMOS Mixed-Signal and RF technology PDK there are seven process corners for MOSFETs, namely: typical-mode (*tm*), worst-speed (*ws*), worst-power (*wp*), worst-one (*wo*), worst-zero (*wz*), slow-slow-fast (*ssf*) and fast-fast-slow (*ffs*). In the *ssf* and *ffs* the first two letters have the standard meaning (first for NMOS, second for PMOS), however, the third is a non-standard and it is related to variations in charge carrier mobility and threshold voltage. The rest of the corner naming conventions are self-explanatory. For MiM capacitor there are three process corners (*ws*, *wp* and *tm*).

TABLE I
Summarized results for the corner analysis ($V_{DD} = [1.62, 1.8, 1.98]\text{V}$, $T = [-45, 27, 85]^\circ\text{C}$)

Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
P_D [μW]	342.4	450.1	394.8	395.6	44.98	< 500	pass
T_0 [dB]	65.41	71.01	69.02	69.73	1.61	> 60	pass
f_u [MHz]	27.57	43.55	34.69	33.23	5.96	> 20	pass
Φ_M [$^\circ$]	44.09	47.28	45.8	45.82	0.76	> 45	near
SLR_p [V/ μs]	33.73	49.54	41.55	41.47	4.98	> 30	pass
SLR_m [V/ μs]	-41.12	-30.18	-35.7	-35.99	3.1	< -30	pass
V_{os} [μV]	-62.56	43.87	-1	-0.5	29.94	< 2000	pass

TABLE II
Summarized results for the 1000 samples Monte-Carlo analysis ($V_{DD} = 1.62\text{V}$, $T = 85^\circ\text{C}$)

Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
P_D [μW]	345.4	362.2	353	352.9	2.44	< 500	pass
T_0 [dB]	61.97	68.43	66.43	66.51	0.78	> 60	pass
f_u [MHz]	27.25	30.09	28.67	28.68	0.47	> 20	pass
Φ_M [$^\circ$]	45	48.78	46.51	46.53	0.55	> 45	pass
SLR_p [V/ μs]	33.67	38.14	35.79	35.8	0.66	> 30	pass
SLR_m [V/ μs]	-33.22	-29.59	-31.44	-31.44	0.59	< -30	near
V_{os} [mV]	-2.44	2.08	$4.81 \cdot 10^{-3}$	$-7.45 \cdot 10^{-3}$	0.72	< 2	near

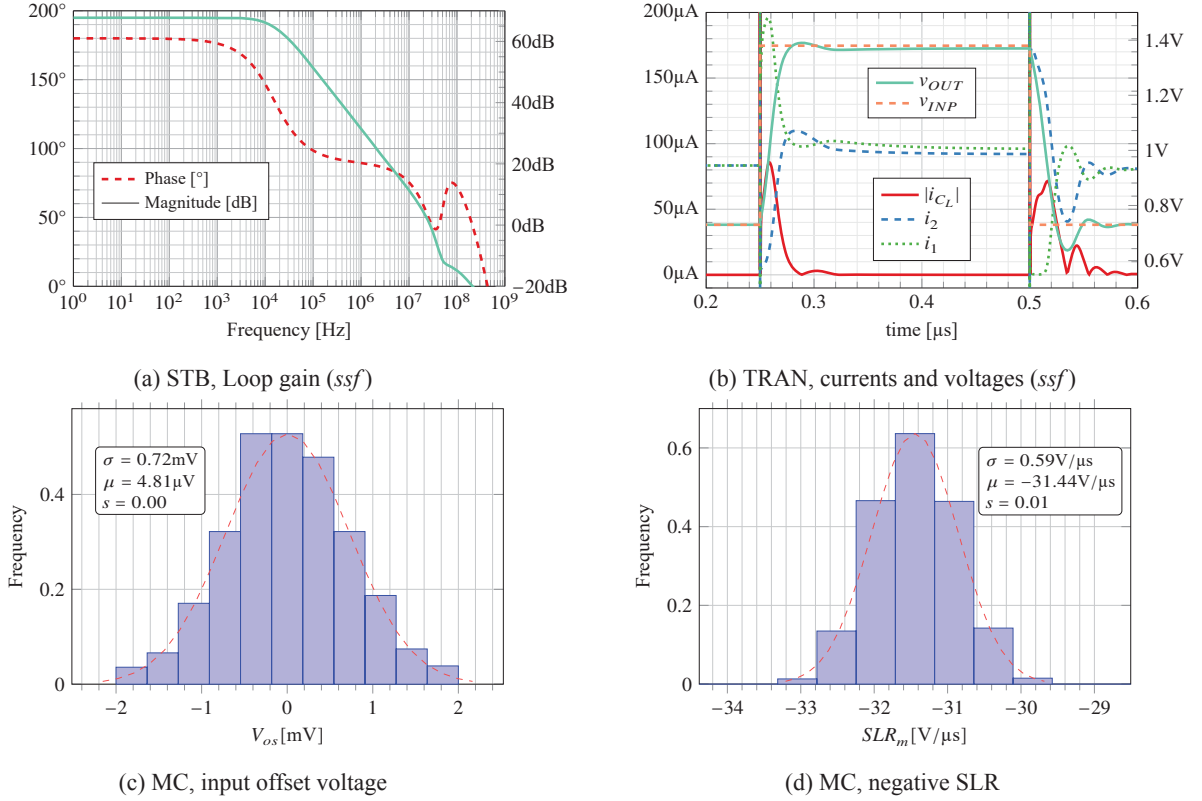


Fig. 3. Results for worst-case ($V_{DD} = 1.62\text{V}$, $T = 85^\circ\text{C}$)

Since the nominal power supply voltage is 1.8V, circuit is simulated with two additional voltage corners representing the edges of the $\pm 10\%$ power supply voltage variation range. These values are 1.62V and 1.98V. Similarly, the edges of the industrial temperature range are chosen for temperature

corners i.e. -40°C and 85°C . Nominal corner is for power supply voltage of 1.8V, 27°C temperature and models for all components in typical-mode (tm).

The circuit is verified for total of 85 corners (84 plus 1 nominal) combining aforementioned component models,

process parameters, temperatures and power supply voltages. Summarized results of the corner analysis are given in Table I. All parameters, except PM, fully passes the tests over simulated corners. The PM is slightly off for the worst-case (WC) corners i.e. the ones with *ssf* MOS-FET models, reduced voltage headroom and high temperature, WC={*ssf*, 1.62V, 85°C}. But, since the PM is near the required value (about 2% relative deviation), the process of further refinement was aborted. Also, there is a borderline negative SLR (SLR_m) for WC corners, as well.

To check for the local (mismatch) and global (process) variations under the worst-case voltage, $V_{DD} = 1.62V$, and temperature, $T = 85^\circ C$, conditions, a thousand samples Monte-Carlo (MC) analysis is performed. In the MC analysis model section for all components is set to *mc*. Summarized results are presented in the Table II. For these conditions negative SLR and input offset voltage are out of the specs. However, there are only 3/1000 MC samples for which the SLR_m is about 1% to 2% off. These deviations are more severe for the input offset voltage (up to 20%) but, again, only in 2/1000 MC samples. These are probably due to the fact that all, mismatch and process, variations are simulated. Therefore, no need for additional interventions in the circuit.

The out-of-spec cases are presented in Fig. 3. In Fig. 3a one can note that the pole-zero doublets are in a proximity of a UGF causing the drop in a PM but no more than the 2% because of the internal compensation scheme. Similarly, in Fig. 3b, there is a slightly less than 60uA output current, $|I_{CL}|$, during the falling edge of output voltage. This drop in output current directly leads to the drop in negative SLR. Practically, for $C_L = 2pF$, and output current smaller than 60uA, the SLR is less than 30V/ μs since, $|SLR_m| \approx I_{CL}/C_L$. In the histograms, given in Fig. 3c and 3d, one can see that the MC samples for which V_{os} and SLR_m parameters are out of specs are statistically sparse (around or beyond the $\pm 3\sigma$).

V. CONCLUSION

In this paper one approach for designing the telescopic (TC) opamp in 180nm CMOS technology is presented. The outline of related work and the motives for performing this design task are given in the introductory part of the paper.

The detailed discussion of the adopted TC topology is given in second section. There, the potential problems related to the practical realization are emphasized and strengths and weaknesses of the chosen topology are discussed with rigour. As a result of a small- and large-signals analysis important, approximate, design equations are derived. Even though, the design process is heavily relied on numerical analysis and simulation, these results are valuable resource for both, bootstrapping the design process iterations and reasoning in which direction to push the design when specs are not met.

Next, in the fourth section, the design procedure is given

and explained. The detailed discussion regarding the practical schematics of the designed circuit and associated test-bench and biasing network is given as well. Finally, the circuit functionality is verified through PVT corner and Monte-Carlo simulations. Results showed that the target circuit parameters are well within the specs for majority of the working and fabrication conditions.

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